FIG. 1

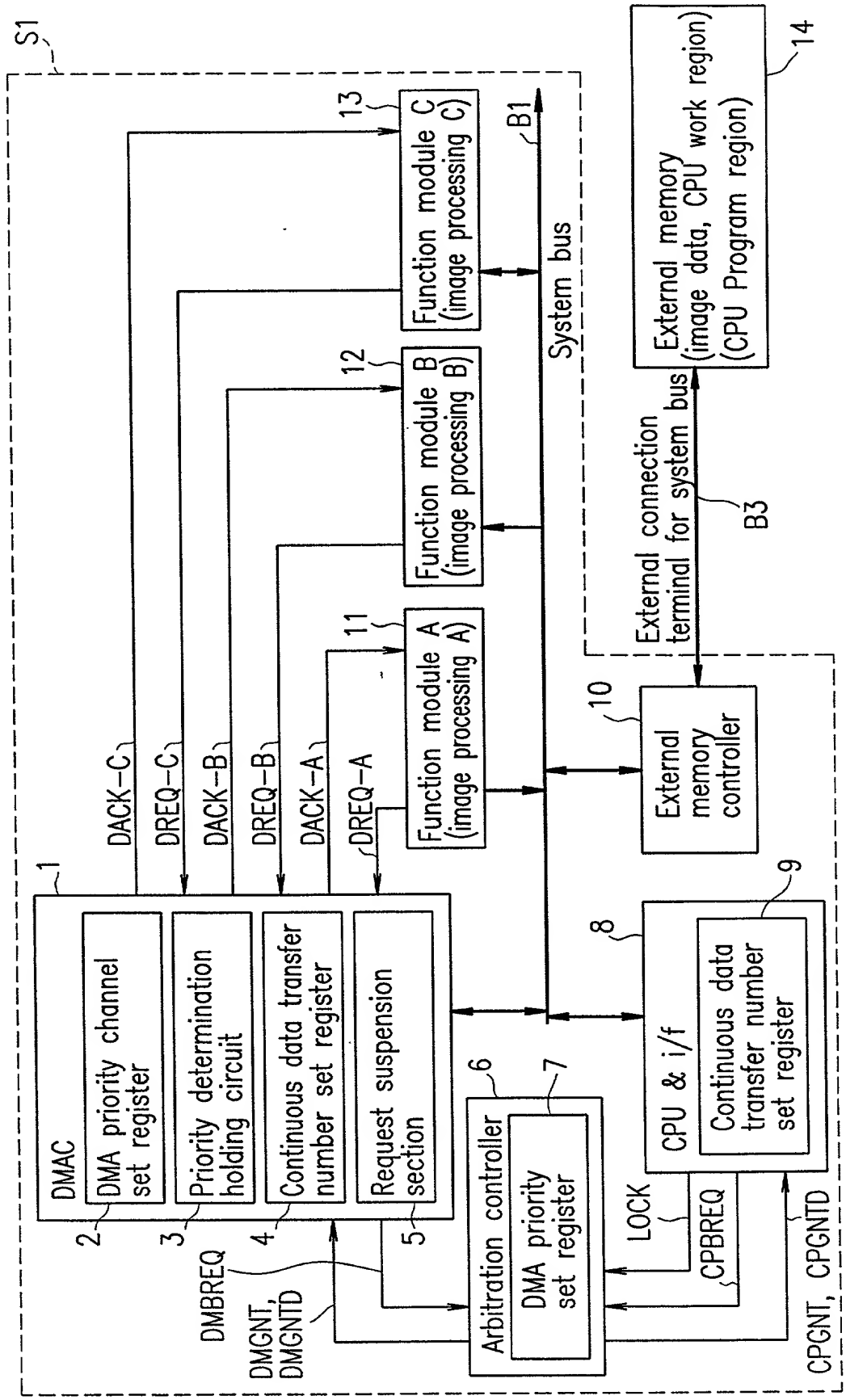
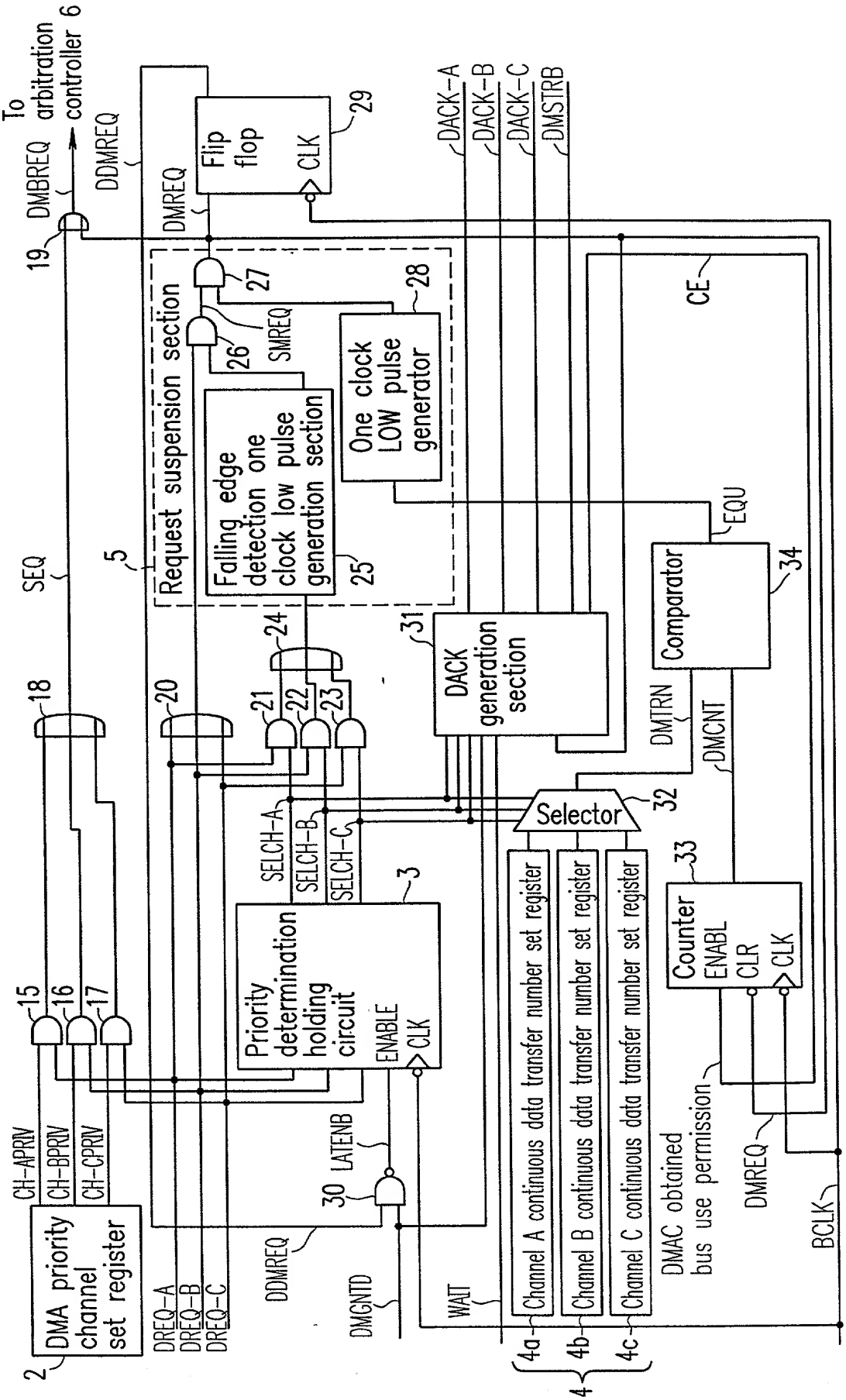


FIG. 2



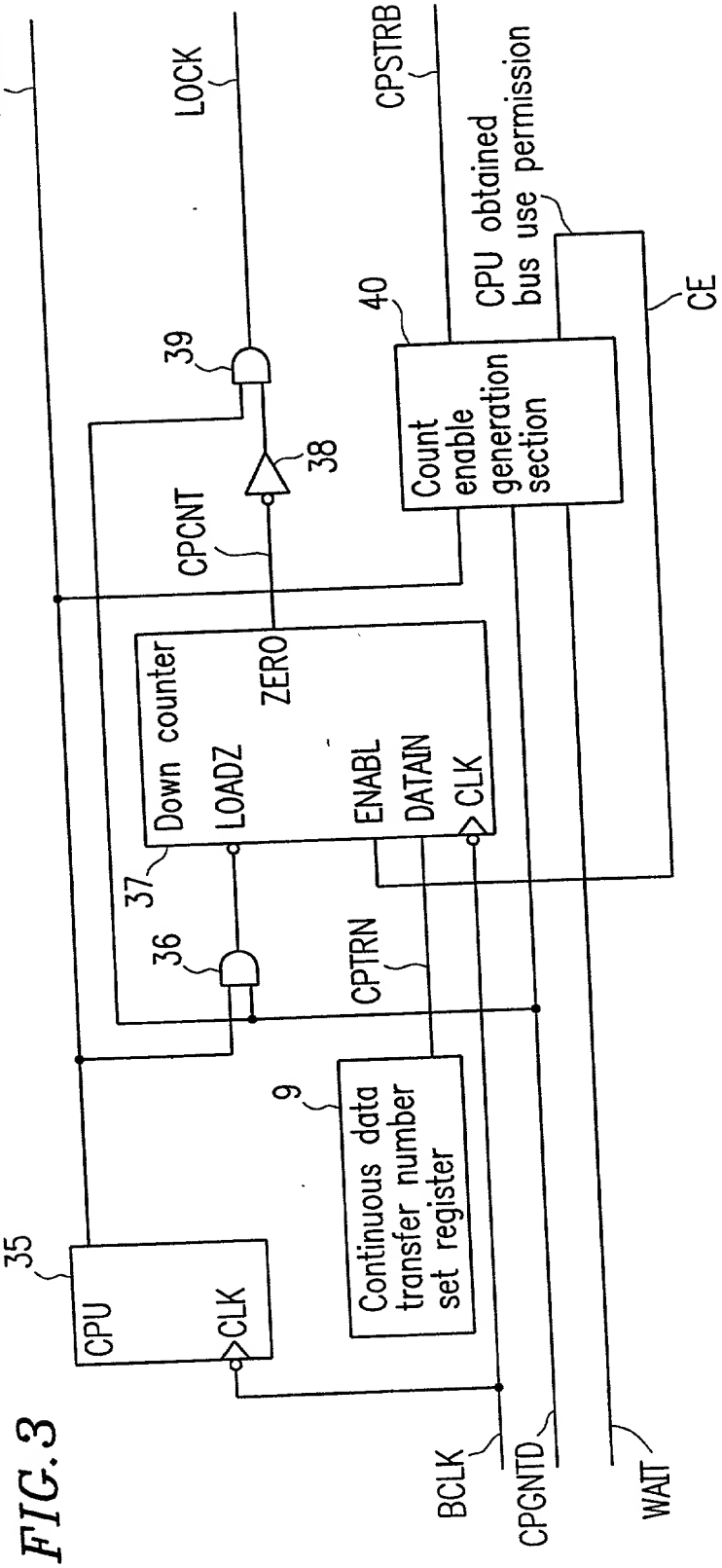

8
CPBREQ
LOCK
CPSTRB
CPU obtained bus use permission
CE
39
38
40
Count enable generation section
CPCNT
Down counter
LOADZ
ZERO
ENABL
DATAIN
CLK
37
36
CPTRN
9
Continuous data transfer number set register
35
CPU
CLK
BCLK
CPGNTD
WAIT

FIG. 3

FIG. 4

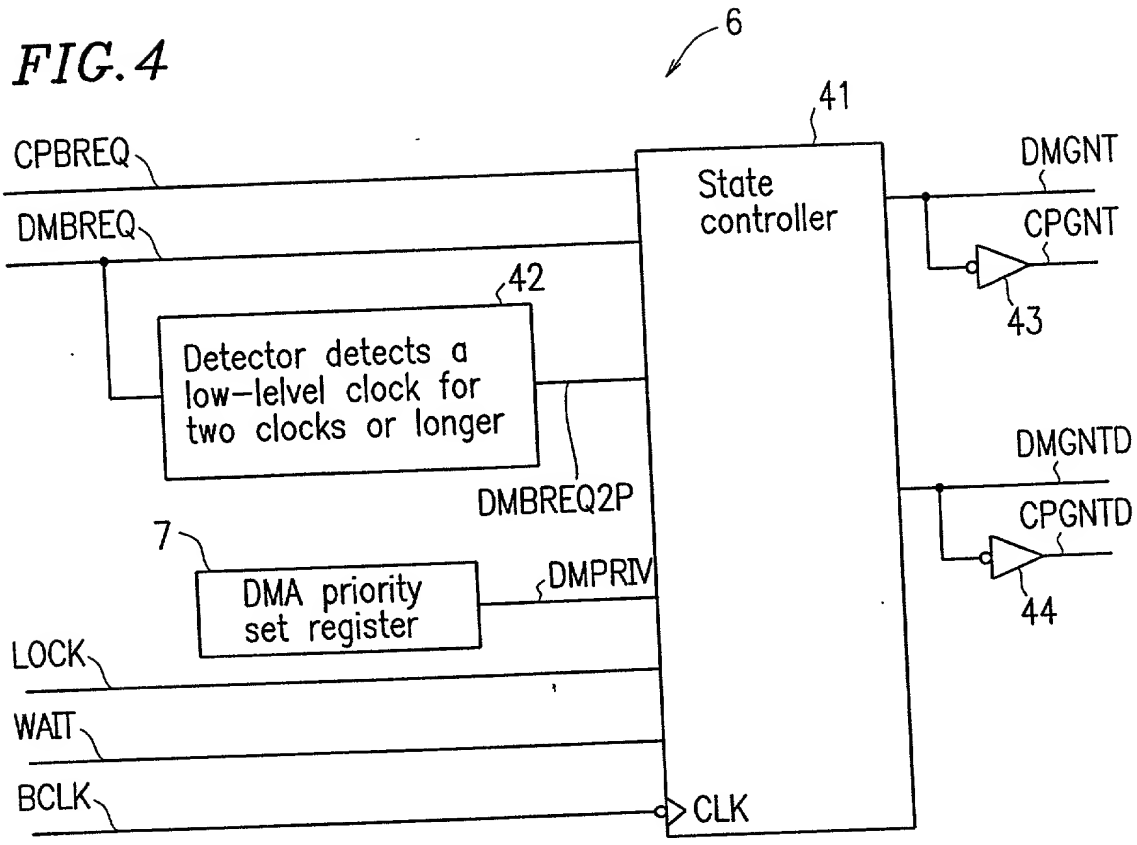
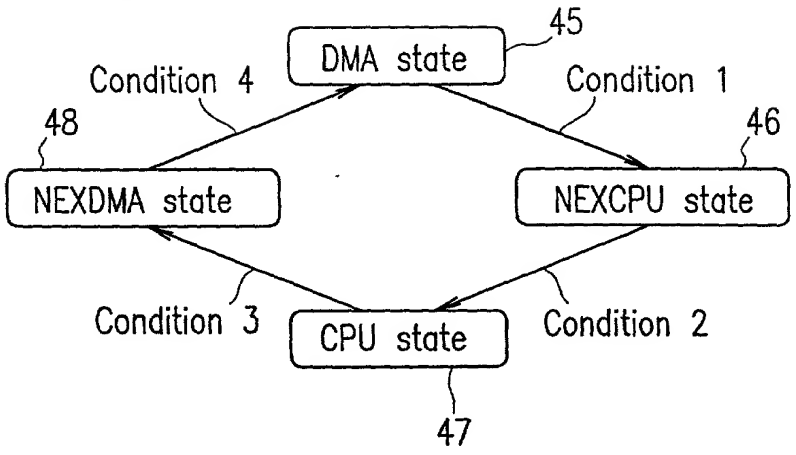


FIG.5



State transition condition
(Transition occurs when each condition is satisfied)

Condition 1: CPBREQ & ((!DMPRIV & !DMBREQ) or (DMPRIV & DMBREQ2P))
Condition 2: !WAIT (not in WAIT state)
Condition 3: DMBREQ
Condition 4: !(LOCK & CPBREQ) & !WAIT (not LOCKed and not in WAIT state)

State Definition
(output levels of signals for each state)

DMA : DMGNT = High, DMGNTD = High
NEXCPU: DMGNT = Low, DMGNTD = High (Bus use permission is transferred to CPU in next cycle)
CPU : DMGNT = Low, DMGNTD = Low
NEXDMA: DMGNT = High, DMGNTD = Low (Bus use permission is transferred to DMAC in next cycle)

[NOTE] Meanings of above symbols are as follows:

& ··· logical multiplication
or ··· logical sum
! ··· inversion of logic

FIG. 6

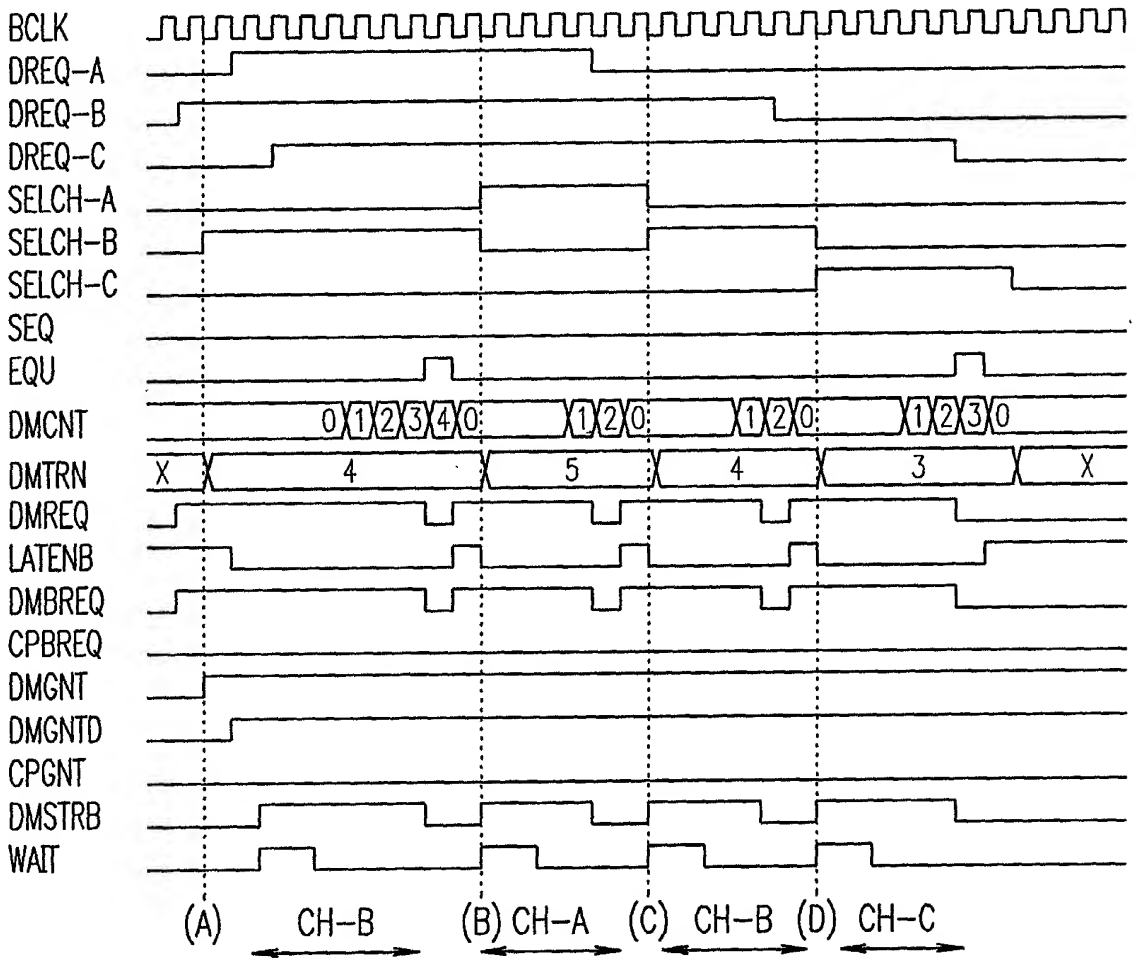


FIG. 7

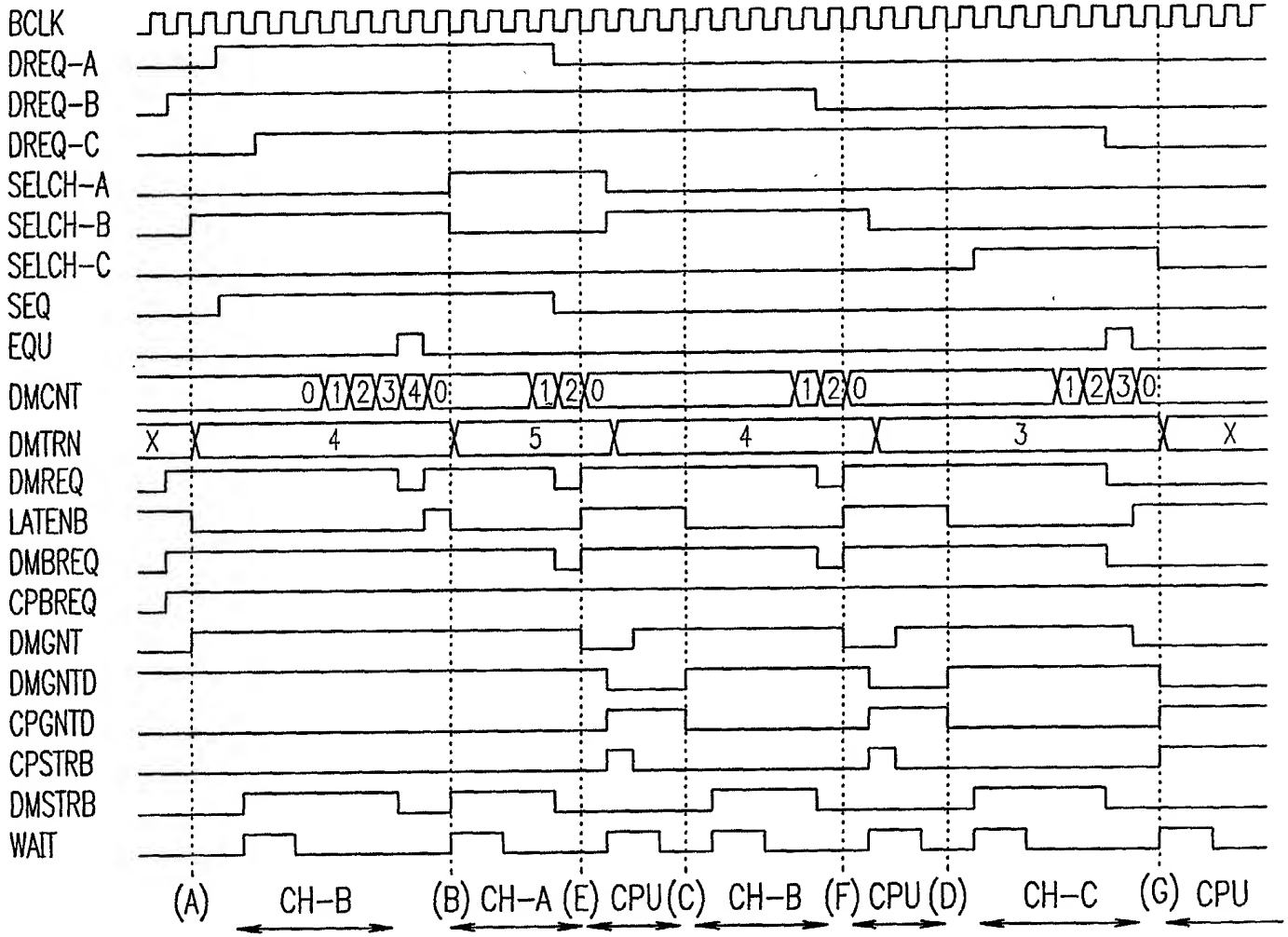


FIG. 8

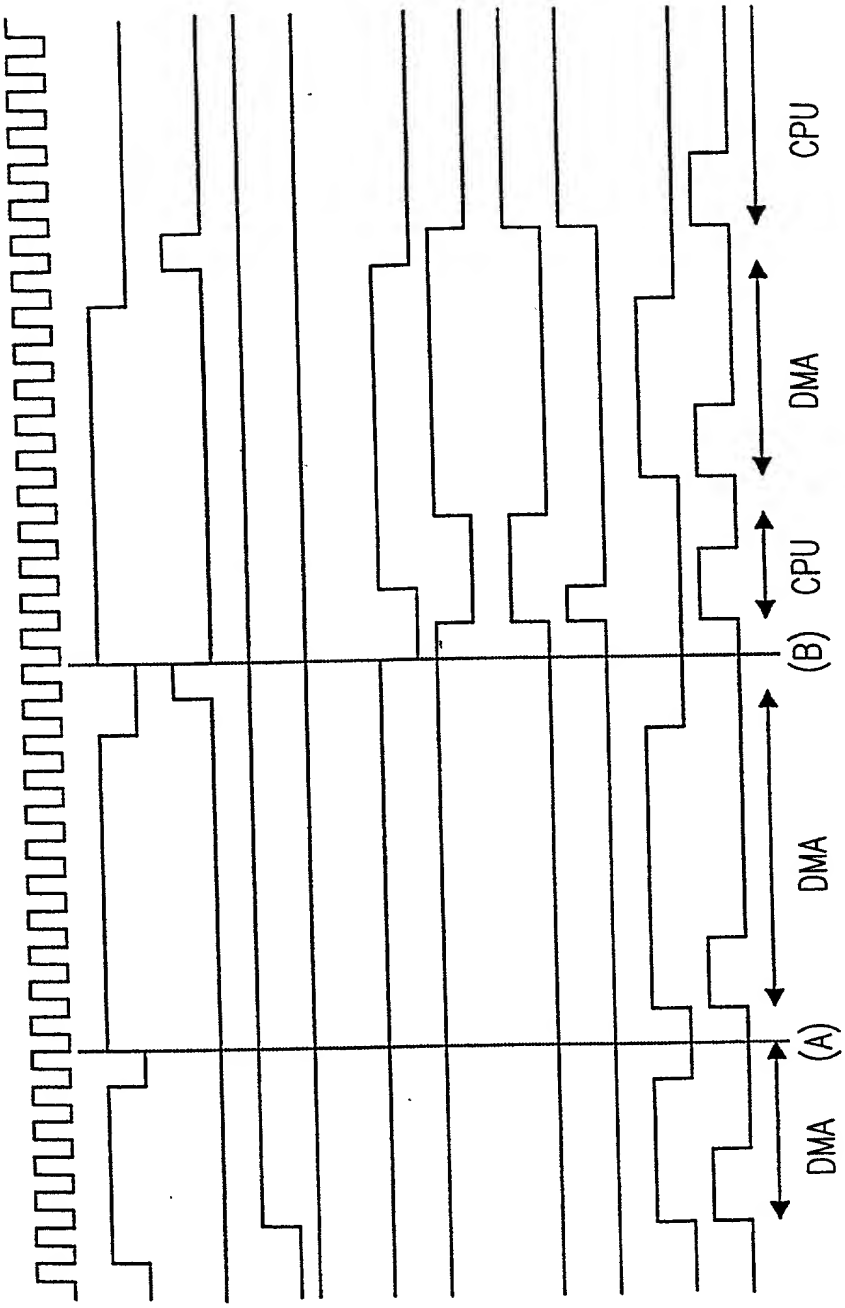


FIG. 9

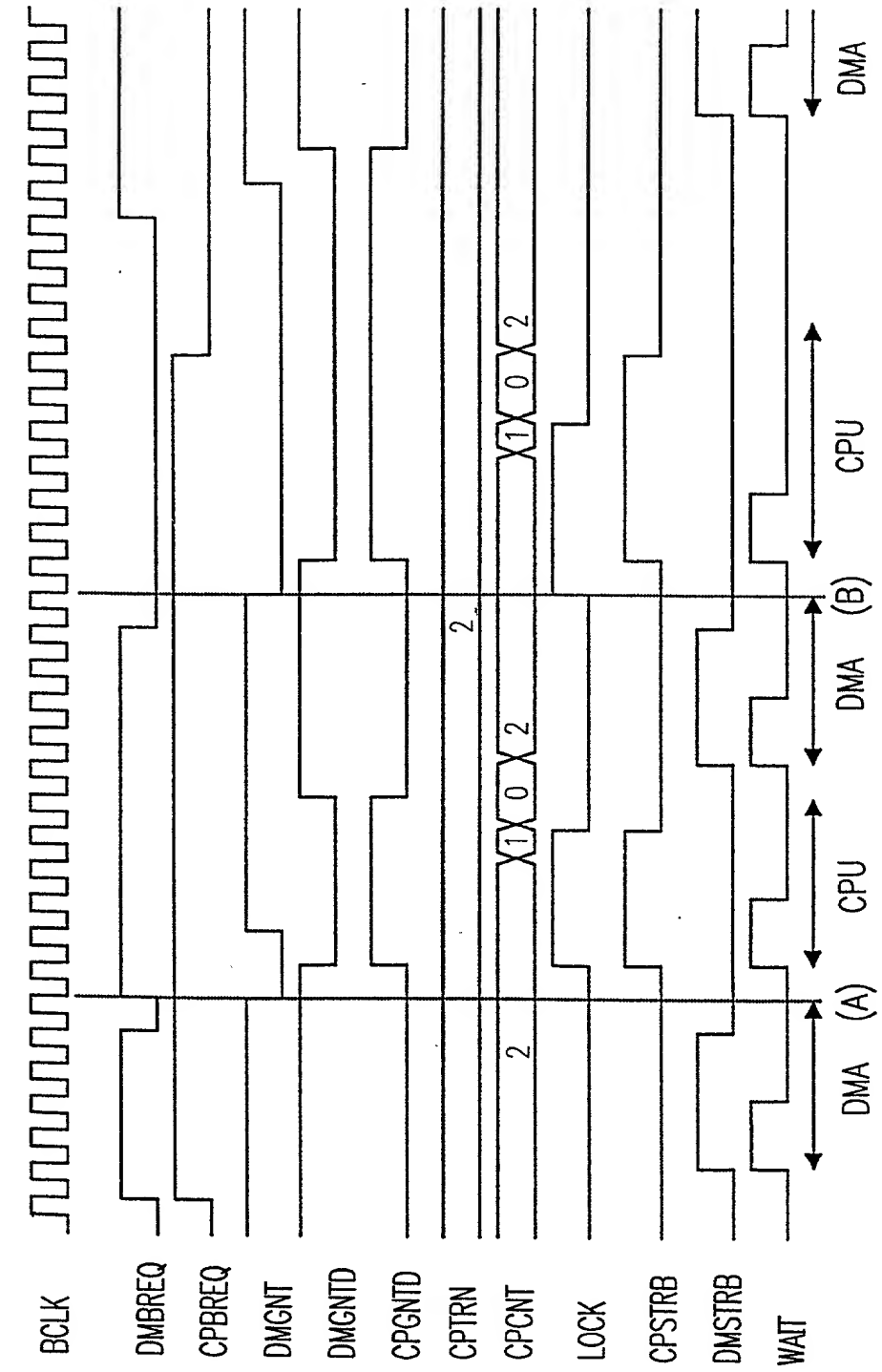

BCLK
DMBREQ
CPBREQ
DMGNT
DMGNTD
CPGNTD
CPTRN
CPCNT
LOCK
CPSTRB
DMSTRB
WAIT
2
X1 X 0 X 2
DMA (A)
CPU
DMA (B)
CPU
DMA

FIG. 10

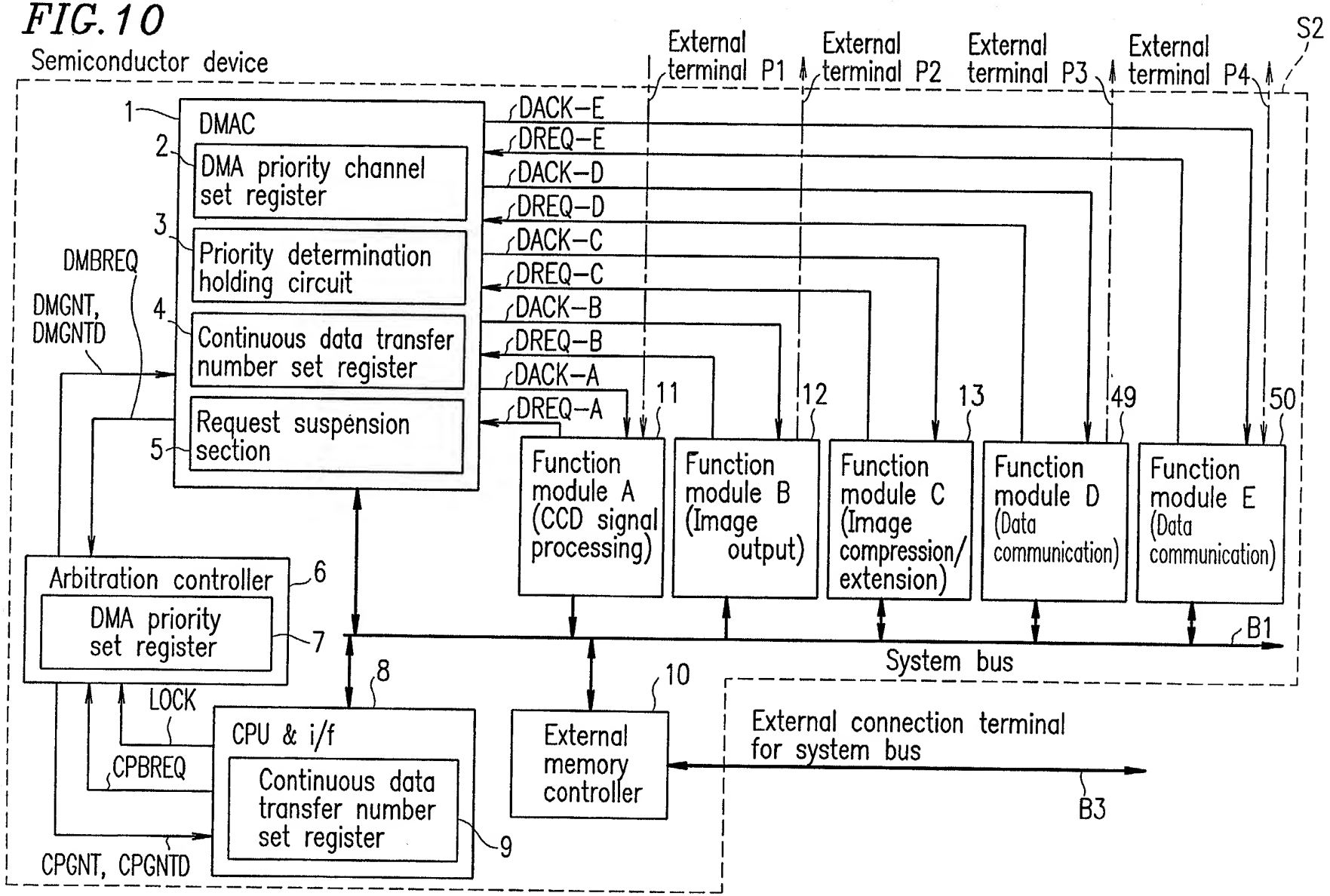


FIG. 11

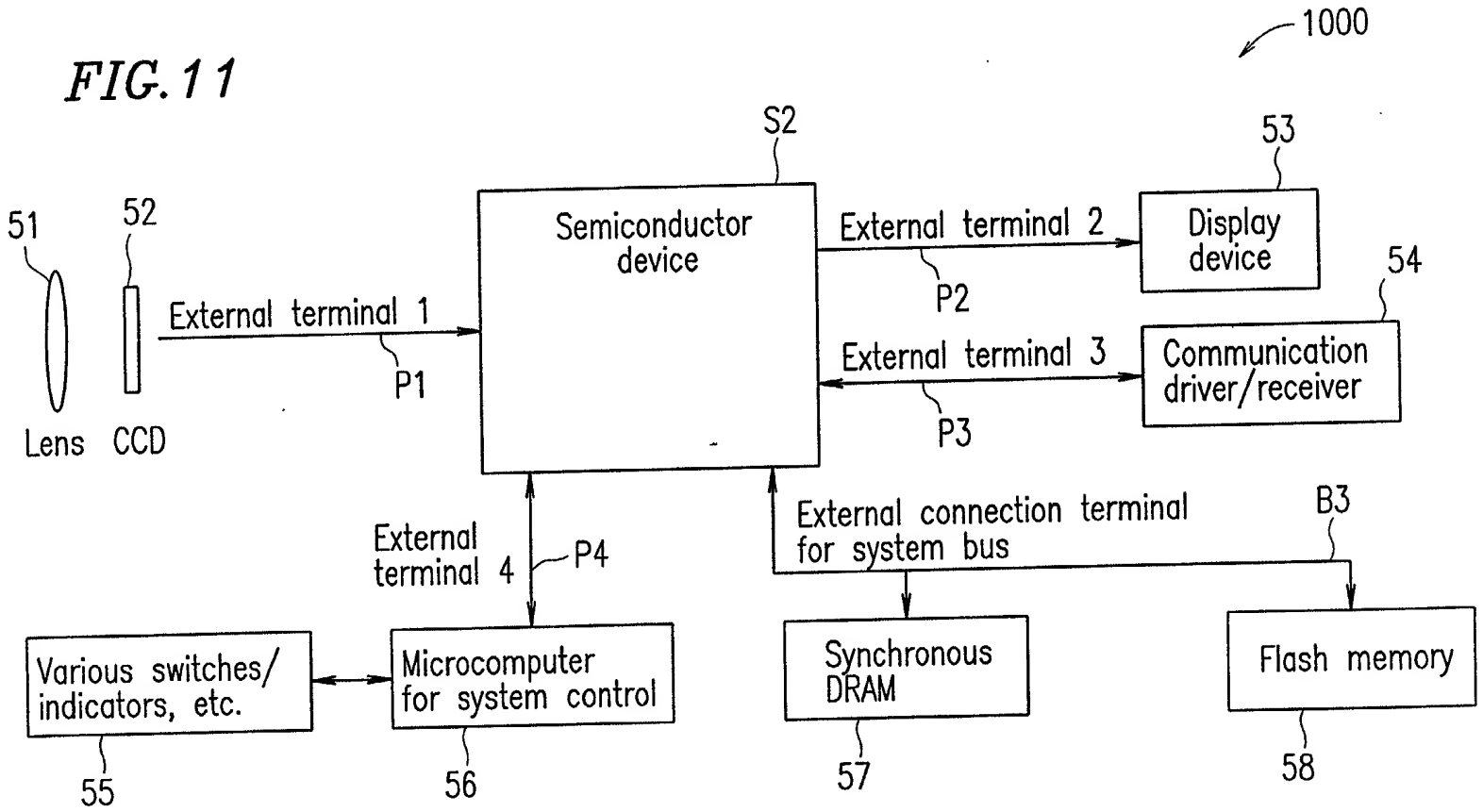
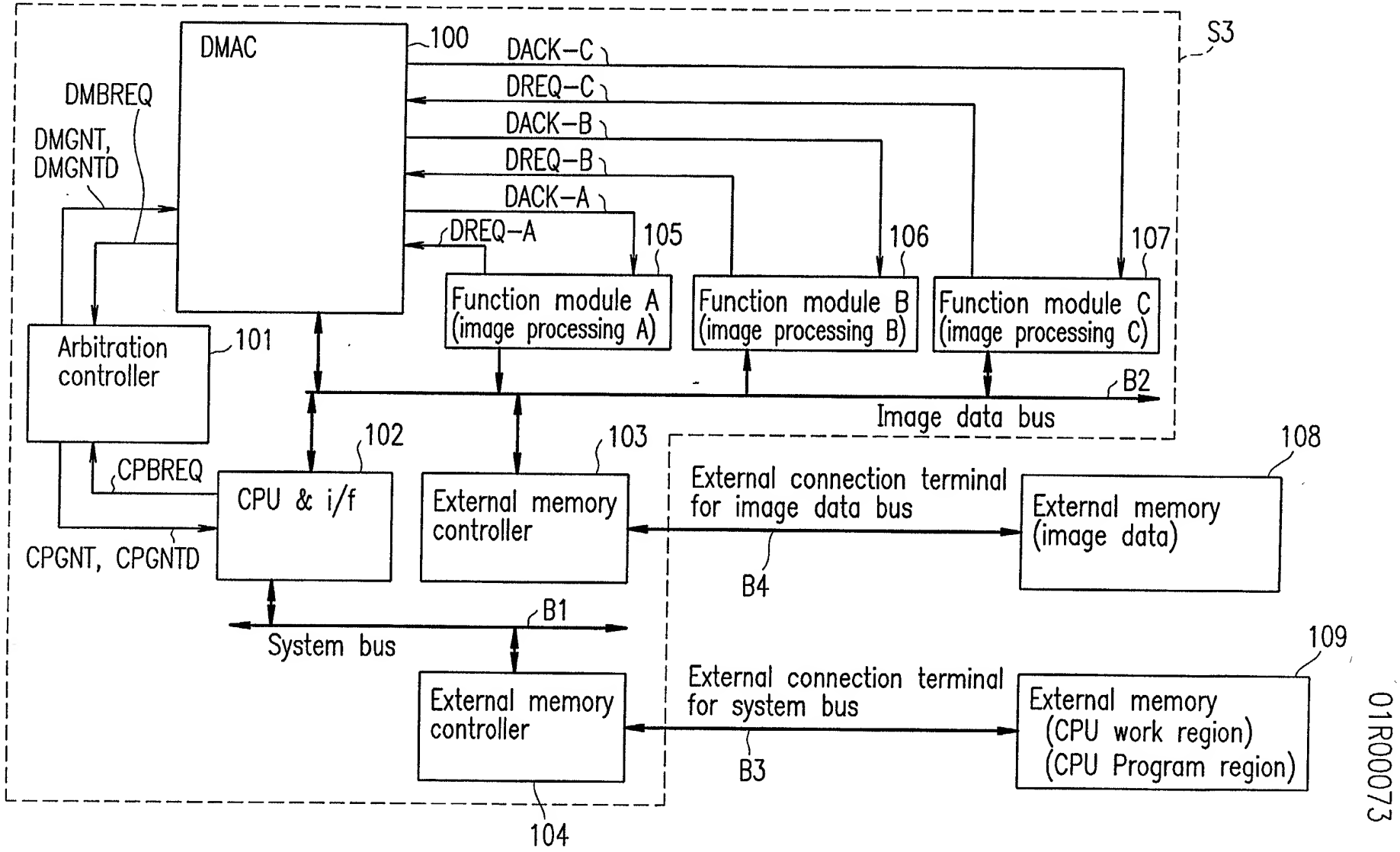


FIG. 12



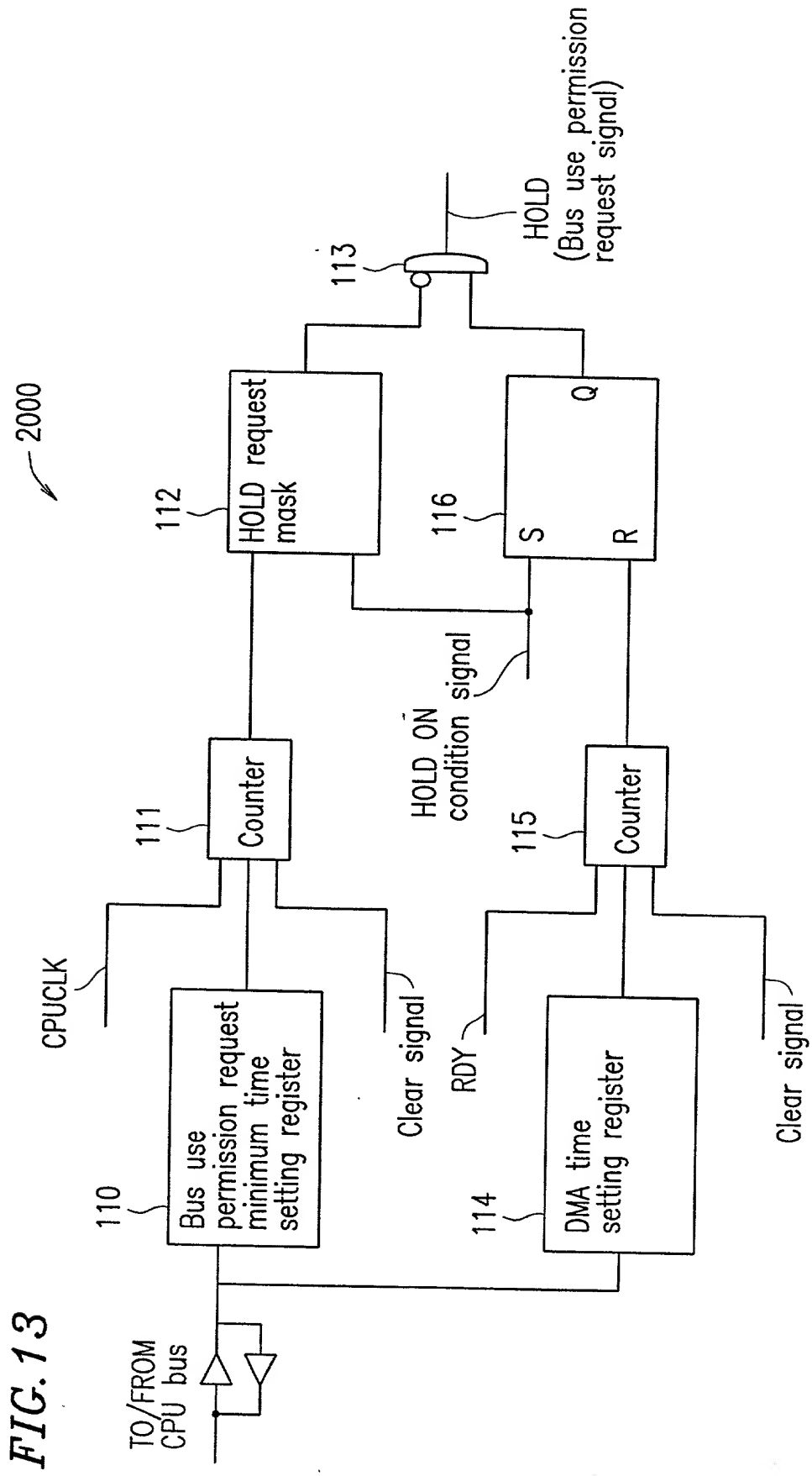
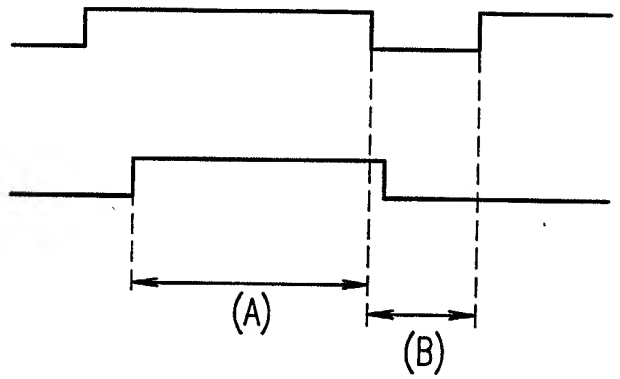


FIG. 13

FIG. 14

(1) HOLD
(bus use permission request signal)

(2) HOLDACK
(bus use permission signal)



(A) DMA transfer time
(CPU or DMAC which has bus use permission uses bus for data transfer)

(B) Bus use permission request minimum time
(time consumed until a bus use permission can be requested after the data transfer during time (A) is completed)